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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,296	08/27/2003	Alexander Tetelbaum	03-0861 81580	6665
7590 10/19/2005			EXAMINER	
LSI Logic Corporation Corporate Legal Department Intellectual Property Services Group 1551 McCarthy Blvd., M/S D-106 Milpitas, CA 95035			SIEK, VUTHE	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

1. This office action is in response to application 10/650,296 and amendment filed on 4/11/2005. Claims 1-18 remain pending in the application.

Claim Objections

2. Claims 1 and 10 are objected to because of the following informalities: in step (b) "...into a timing group" should be --...into timing groups--, in order to provide proper antecedent basic for the following limitation "wherein each timing group...". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-2, 5-9, 10-11 and 14-18 are rejected under 35 U.S.C. 102(a/e) as being anticipated by Lu et al. (6,550,045).

5. As to claims 1 and 10, Lu et al. teach a method of cell placement and clock tree synthesis (see summary, Fig. 1, 3-7 and its description) comprising the steps of

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identifying critical paths in an IC design (data logic path having timing information affecting clock network timing, timing violations) (at least see summary; col. 4); partitioning the IC design into a timing group (at see summary; col. 3-4, Fig. 1, 6, where Fig. 1 shows two groups of critical paths, first group from clock source to Fi through data logics and to Fj; second group from clock source to Fj through data logics to Fk; the two groups are critical paths because they are violated timing; col. 4 lines 16-30 describes Djk is the worst case delay along data logics path 32; this means that Djk is critical path; thus Lu et al. teach grouping only critical paths because Fig. 1 shows only paths having timing violation which are critical paths); assigning each flip-flop to a critical path (Fig. 1, 6); performing a cell placement a minimizing a function of propagation delay and maximum distance between flip-flops within each timing group and constructing a clock sub-net for each timing group (Fig. 1, 6 and its description; col. 6 describes path delays that are critical because they are violated timing and they are needed to be fixed by inserting delay element; delay paths within group of clock domains violated timing, thus they are critical paths). Lu et al. teach that maximal path delay between flip-flops represent both clock path and delay path between the flip-flops, this path delay is critical path and need to be fixed because this delay path violated timing (see col. 4 and 6). This clearly suggests that maximal path delay must be minimized in order to minimize clock skews. The teachings of Lu are anticipated the claimed limitations.

6. As to claims 2, 5-9, 11 and 14-18, Lu et al. teach substantially similar claimed limitations of each timing group contains only flip-flops (Figs. 1 and 6); assigning the flip-flops in a critical path to a timing group (Figs. 1 and 6); coupling buffer is equidistant

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from each flip-flop in the timing group and coupling a clock signal to the clock buffer from a clock tree to balance clock tree (insertion buffer must be equidistant from each flip-flop in the timing group in order to balance clock tree, synchronize all clock domains and to meet timing constraints; see at least Figs. 1 and 6).

Allowable Subject Matter

7. Claims 3-4 and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art does not teach or fairly suggest replacing a flip-flop in a critical path with a flip-flop in a non-critical path connected to the critical path.

Remarks

8. Applicant argued that Lu does not teach grouping only critical paths. As clearly described in the above rejection, the teachings of the Lu suggest grouping only critical paths because they are violated timing and they are needed to be fixed by inserting delay elements. Fig. 1 and 6 clearly show grouping delay paths into timing group(s) having only critical paths, because the Figures only show delay paths that are violated timing and they are needed to be fixed by inserting delay elements. The flip-flops are placed closed to each other to minimize the delay path. These delay paths are violated timing and they needed to be fixed because they are critical paths.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

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A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER